REMARKS

Claims 1-21 are pending in this application. Claims 1-12 were rejected under 35 U.S.C. §112, first paragraph as failing to comply with the written description. Claims 1-12 and 21 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 1-21 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,005,812 (Mullarkey).

Please accept amended FIG. 4 as attached hereto. FIG. 4 has been amended to make the circuit shown in FIG. 4 conform with the description given on page 8 of the specification. No new matter has been added.

Regarding the rejection of Claims 1-12 under §112, first paragraph, the Examiner states that the specification fails to adequately describe the circuit of FIG. 4. Moreover, regarding the Examiner's statement "V_H is provided to the regulator system" is to be understood as "a voltage having a level equal to V_H less the threshold drops of pFET transistors F1 and F2 will be provided to the system 412," the specification and FIG. 4 have been amended to overcome the Examiner's rejections. Accordingly, it is respectfully requested that the Examiner withdraw the §112, first paragraph, rejections of Claims 1-12.

Regarding the rejection of Claims 1-12 under §112, second paragraph, the Examiner states that there is no support found in the specification for the statement "the pump control signal being based on the clock control signal." Claim 1 has been amended to comply with the

Examiner's recommendation. Accordingly, it is respectfully requested that the Examiner withdraw the §112, second paragraph, rejections of Claims 1-12.

Regarding the Examiner's rejection of independent Claim 1 under §102(b) as being anticipated by Mullarkey, Applicants respectfully submit that Mullarkey fails to teach or suggest all the elements of amended Claim 1. Specifically, Mullarkey fails to teach or suggest "at least one regulator system incorporated in the local DC voltage generator, a power control unit and a clock control unit, wherein each regulator system receives a power control signal from said power control unit and a clock control signal from said clock control unit and outputs a pump control signal from the local DC voltage generator, the pump control signal being based on *a reference voltage supplied to the at least one regulator system, the power control signal being enabled and disabled in response to* at least the clock control signal" as recited in Claim 1 of the present application. Moreover, the present invention is directed to a system on chip (SOC) design, having a plurality of subsystems, each of the subsystems having a plurality of units, and at least two of the units located in at least one of the subsystems being different from each other. The above elements are not taught by Mullarkey. At least for the above-noted reasons, Claim 1 is allowable.

In addition to the above, Mullarkey discloses a device and method for applying current to a semiconductor memory to support a boosted voltage within the memory during testing. The Examiner equates "the regulator system" as recited in Claim 1 with the switching circuit 24 and the voltage regulator 14 as taught by Mullarkey, equates the "pump control signal" as recited in Claim 1 with the REGDIS* signal as taught by Mullarkey, and equates the "the *clock control*

signal" as recited in Claim 1 with the CLK signal as taught by Mullarkey. It is submitted that Mullarkey teaches *in response to the oscillator activation signal REGDIS*, a conventional ring oscillator 16 outputs a clock signal CLK* that activates a conventional charge pump (Column 2, Lines 58-61; and FIG. 1). Moreover, the REGDIS* signal is output by the voltage regulator 14 when the voltage regulator senses a drop in voltage. In other words, the CLK control signal is output by the conventional ring oscillator 16 *after the voltage regulator 14 senses a drop in voltage.* In contrast, as recited in Claim 1, the clock control signal is output from the clock control unit.

Moreover, because the CLK signal as taught by Mullarkey is output by the conventional ring oscillator 16 after receiving the REGDIS* signal which is activated when the voltage regulator 14 senses a drop in voltage, it is clearly seen that the *CLK signal is based on the REGDIS* signal* (See FIG. 1). In contrast, amended Claim 1 includes the recitation that each regulator system receives a power control signal from said power control unit and a clock control signal from said clock control unit and outputs a pump control signal from the local DC voltage generator, the pump control signal being based on *a reference voltage supplied to the at least one regulator system, the pump control signal being enabled and disabled in response to* at least the clock control signal, which is neither taught nor suggested by Mullarkey. In view of the above, Claim 1 is believed to be in condition for allowance.

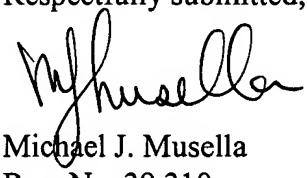
Regarding the Examiner's rejection of independent Claim 13 under §102(b), Claim 13 has been amended to include the recitation "supplying a clock control signal to each of the local DC voltage *generators and generating a reference voltage based on at least the clock control*

signal; generating, in a section of each local DC voltage generator, *a pump control signal based on the reference voltage"*, which is neither taught nor disclosed by Mullarkey. Claim 13 is allowable at least for similar reasons set forth above with respect to Claim 1 in addition to its own independently recited claim features.

Without conceding the patentability of independent Claims 2-12 and 14-21, it is respectfully submitted that they are believed to be allowable by their virtue of their dependence upon independent Claims 1 and 13, respectively.

Should the Examiner believe that a telephone conference or a personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



Michael J. Musella
Reg. No. 39,310
Attorney for Applicant(s)

DILWORTH & BARRESE
333 Earle Ovington Blvd.
Uniondale, NY 11553
(516) 228-8484
(516) 228-8516 (FAX)

IN THE DRAWINGS

Please replace FIG. 4 with the attached sheet.